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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,722	11/25/2003	Michael O'Connor	884.398US2	5763

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EXAMINER	
TRINH, MICHAEL MANH	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,722	O'CONNOR ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-8,10,11,14,16-22,24,26 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-8,10-11,14,16-22,24,26-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's Amendment filed November 03, 2005.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102 and/or 103

1. Claims 1-4,6-8,10-11,14,16-22,24,26-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Dahl et al (2002/0130407), or, in the alternative, under 35 U.S.C. 103(a) as obvious over Dahl et al (2002/0130407) taken with Tachikawa (Title "Assembly and Packaging", pp 530-584, 1986).

Re base claims 1,6,10,16,21,26, Dahl teaches a method of cooling a semiconductor chip, comprising: providing a number of electrical devices on a semiconductor layer of a semiconductor chip 601 (Figs 6A-6C; paragraphs 0115-0121,0136-0141); integrally forming a substantially planar heat transfer conducting layer 620 on the backside surface of the semiconductor chip 601 (Figs 6B-6C, paragraphs 0120-0123), with the semiconductor layer of the semiconductor chip 601, wherein the heat conducting layer 620 is compatible with semiconductor processing techniques, wherein the heat conducting layer of diamond has thermal conductivity higher than the semiconductor layer (paragraphs 0120-0123;0131); conducting heat generated by the number of electrical devices into the heat conducting layer; and transmitting the heat generated by the number of electrical devices through the heat conducting layer 620 from a first region having a first temperature to a second region of a heat sink 610 (Figs 6B-6C; paragraphs 0120) having a second temperature that is lower than the first region; wherein heat is transmitting through a substantially continuous interface between the conducting layer 620 and an external heat sink 610 (Figs 6B-6C, paragraphs 0120-0123,0116-0119). Re further claim 10, as described above, wherein the heating transfer conducting layer 620 comprising a diamond containing layer is integrally formed on the backside surface of the semiconductor chip 601 (paragraphs 0122;0138; Figs 6A-6C), wherein heat generated by the electrical devices are spreading in a first area through the heat transfer conducting layer 620 of diamond containing layer to a larger second area wherein heat per unit area is reduced. Re further claims 16,21,26, wherein the method comprises fabricating a semiconductor layer; forming a number of electrical devices on the semiconductor layer; electrically connecting the

number of electrical devices (Fig 9, paragraphs 0136-0141; and Figs 6A-6C, paragraphs 0115-0122), wherein the heat transfer conducting layer 620/910/911 comprises a diamond containing layer (paragraphs 0120-0122,0141), wherein, re further claim 26, the integrated circuit packaging includes the semiconductor chip coupling to memory, logic and microprocessing devices (paragraphs 0116) and wherein the memory includes a random access memory (paragraphs 0141); and coupling an external heat sink 610 to the heat conducting layer 620 to form a substantially continuous interface. Re claim 2, wherein the electrical devices include a number of transistors (paragraphs 0115,0136-0137). Re claims 3,7,18, wherein the heat transfer conducting layer comprises a carbon-containing layer (paragraphs 0005-0020). Re claims 4,8,19, wherein the heat transfer conducting layer comprises a diamond containing layer (paragraphs 0120-0122; 0005-0020). Re further claim 11, wherein the electrical devices include a number of transistors (paragraphs 0115,0136-0137). Re claim 14,24, wherein the diamond containing layer 620 (Fig 6B-6C; paragraphs 0120-0124,0122) is formed on a back side of the semiconductor chip 601 by chemical vapor deposition. Re claim 17, wherein the semiconductor layer includes a silicon substrate (paragraphs 0136-0137;0115-0122). Re claim 20, wherein the diamond containing layer includes chemical vapor depositing a diamond layer (paragraphs 0122,0138,0103-0108). Re claims 22,27, wherein the electrical devices include a number of transistors on a silicon substrate (paragraphs 0115,0136-0137).

Regarding a flip-chip configuration semiconductor chip: Applicant alleged that, "the configuration in Dahl appears drawn to lead frame package configurations as discussed in Dahl in paragraph 0119. However, Applicant is unable to find in Dahl, a teaching of providing a flip-chip configuration semiconductor chip...". In response, this is noted and found unconvincing, Dahl described and incorporated in paragraphs 0116-0119 about the teaching of T. Tachikawa in a chapter entitled "Assembly and Packaging" pp 530-586, for preparing of integrated circuit (IC) chip for use in packaging. Accordingly, under 35 USC 102 rejection, in addition to the lead frame package configuration as shown in Figure 38 at page 580 and Figure 26 at page 563 of Tachikawa, a flip-chip configuration semiconductor chip is also described and shown in Figures 36-37 at page 579-580 of Tachikawa as mentioned by Dahl. Furthermore, under 35 USC 103 rejection, it would have been also obvious to one of ordinary skill in the art at the time the invention was made to employ the novel use of diamond-containing layer on the backside

surface of Dahl in both flip-chip and lead frame configurations as taught by Tachikawa. This is because of the desirability to cool and reduce transistor junction temperature of the flip-chip configuration semiconductor chi[, and transmitting the heat away in an effective manner since the diamond-containing layer is a material having very high thermal conductivity.

Claim Rejections - 35 USC § 102

2. Claims 1,3-4,6-8,10,16-19,21 are rejected under 35 U.S.C. 102(b) as being anticipated by Anschel et al (4,914,551).

Re base claims 1,6,10,16,21: Anschel teaches a method of cooling a semiconductor chip, comprising: providing a number of electrical devices on a semiconductor layer of a flip-chip configuration semiconductor chip 17 (Figs 1-2; col 2, line 23 through col 5; col 1, lines 14-40); integrally forming a substantially planar heat transfer conducting layer 41 on the backside surface of the semiconductor chip 17 (Figs 2,1), wherein the heat conducting layer 41 of diamond containing layer (diamond-filled layer) is compatible with semiconductor processing techniques, wherein the heat conducting layer of diamond containing layer 41 has thermal conductivity higher than the semiconductor layer (col 43, line 3 through col 4, line 23); conducting heat generated by the number of electrical devices into the heat conducting layer; and transmitting the heat generated by the number of electrical devices through the heat conducting layer 41 comprising the diamond containing layer from a first region having a first temperature to a second region of a heat sink 37,33 (Figs 1,2) having a second temperature that is lower than the first region; wherein heat is transmitting through a substantially continuous interface between the conducting layer 41 comprising the diamond containing layer and an external heat sink 33/37 (col 4, line 24 through col 5, line 65). Re further claim 10, as described above, wherein the heating transfer conducting layer 41 comprising a diamond containing layer is integrally formed on the backside surface of the semiconductor chip 17 (Fig 2,1; col 3, line 59 through col 4, line 23; col 5, lines 26-55), wherein heat generated by the electrical devices are spreading in a first area through the heat transfer conducting layer of diamond containing layer 41 to a larger second area wherein heat per unit area is reduced. Re further claims 16,21, wherein the method comprises fabricating a semiconductor layer; forming

a number of electrical devices on the semiconductor layer; electrically connecting the number of electrical devices as in computer industry (col 1, lines 14-40), wherein the heat transfer conducting layer 41 comprises a diamond containing layer (col 3, line 59 through col 4, line 23; col 5, lines 26-55); and coupling an external heat sink 37/33 to the heat conducting layer 41 to form a substantially continuous interface. Re claims 3,4,7,8,18,19, wherein the heat transfer conducting layer comprises a carbon-containing layer of the diamond containing layer 41 (col 3, line 59 through col 4, lines 23). Re claim 17, wherein the semiconductor layer includes a silicon substrate (col 2, lines 30-32).

Claim Rejections - 35 USC § 103

3. Claims 2,11,22,26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anschel et al (4,914,551) taken with Bertin et al (6,255,899).

Anschel teaches a method of cooling a semiconductor chip as applied to claims 1,3-4, 6-8,10,16-19,21 above. Re further claim 26, Anschel teaches employing the electrical devices in the computer industry.

Re claims 2,11,22,26, Anschel lacks mentioning transistors, and, re further claim 26, forming an electronic system by coupling the processor chip to a random access memory.

However, Bertin teaches forming an electronic system by coupling the semiconductor processor chip 112 to a random access memory (RAM) 114,116 (112 in Fig 1A; col 2, line 55 through col 3; chip 146 and RAM 148 in Figs 1C-1D; col 4, line 52 through col 5, lines 8), wherein the electrical devices include a number of transistors such as CMOS (Figs 3B; col 8, lines 1-35).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form an integrated circuit packaging of Linn by coupling the processor chip including transistors to a random access memory, as taught by Bertin. This is because of the desirability to form an electronic system such as a computer for processing software applications.

Response to Amendment

4. Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

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Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).
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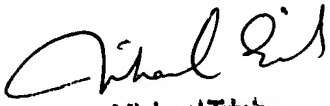

Michael Trinh
Primary Examiner